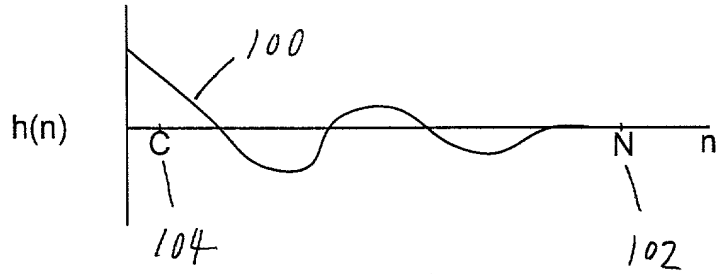

Figure 1A

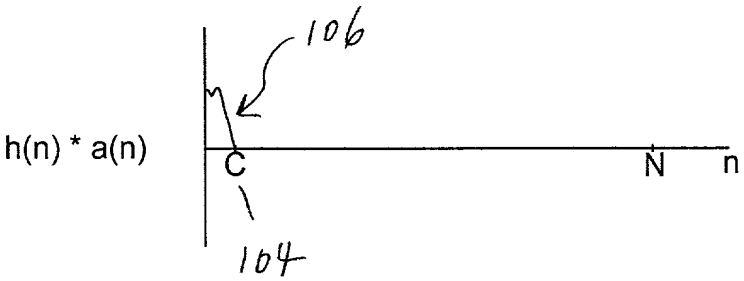

Figure 1B

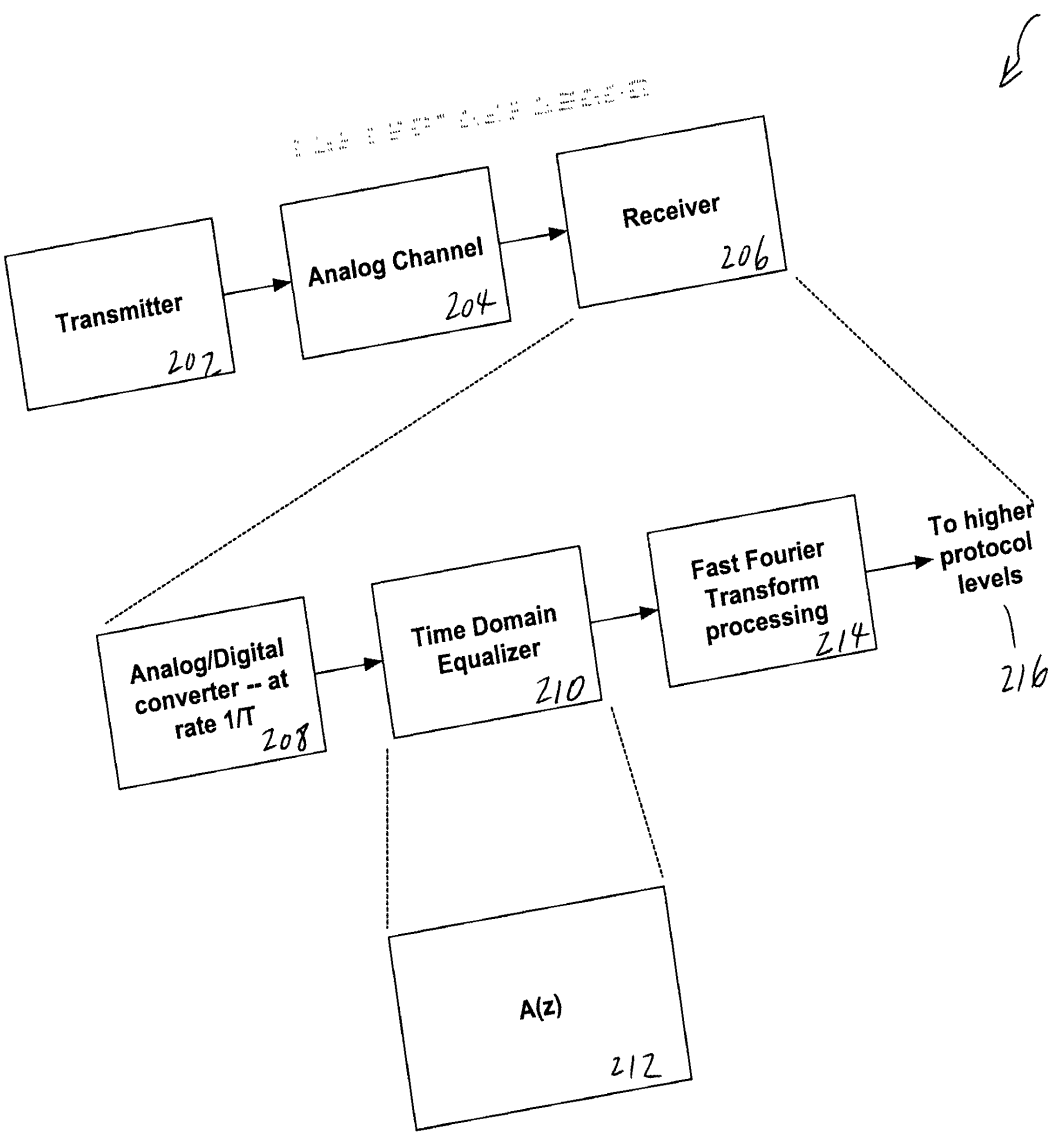
200
Transmitter
202
Analog Channel
204
Receiver
206
Analog/Digital converter -- at rate 1/T
208
Time Domain Equalizer
210
A(z)
212
Fast Fourier Transform processing
214
To higher protocol levels
216

Figure 2

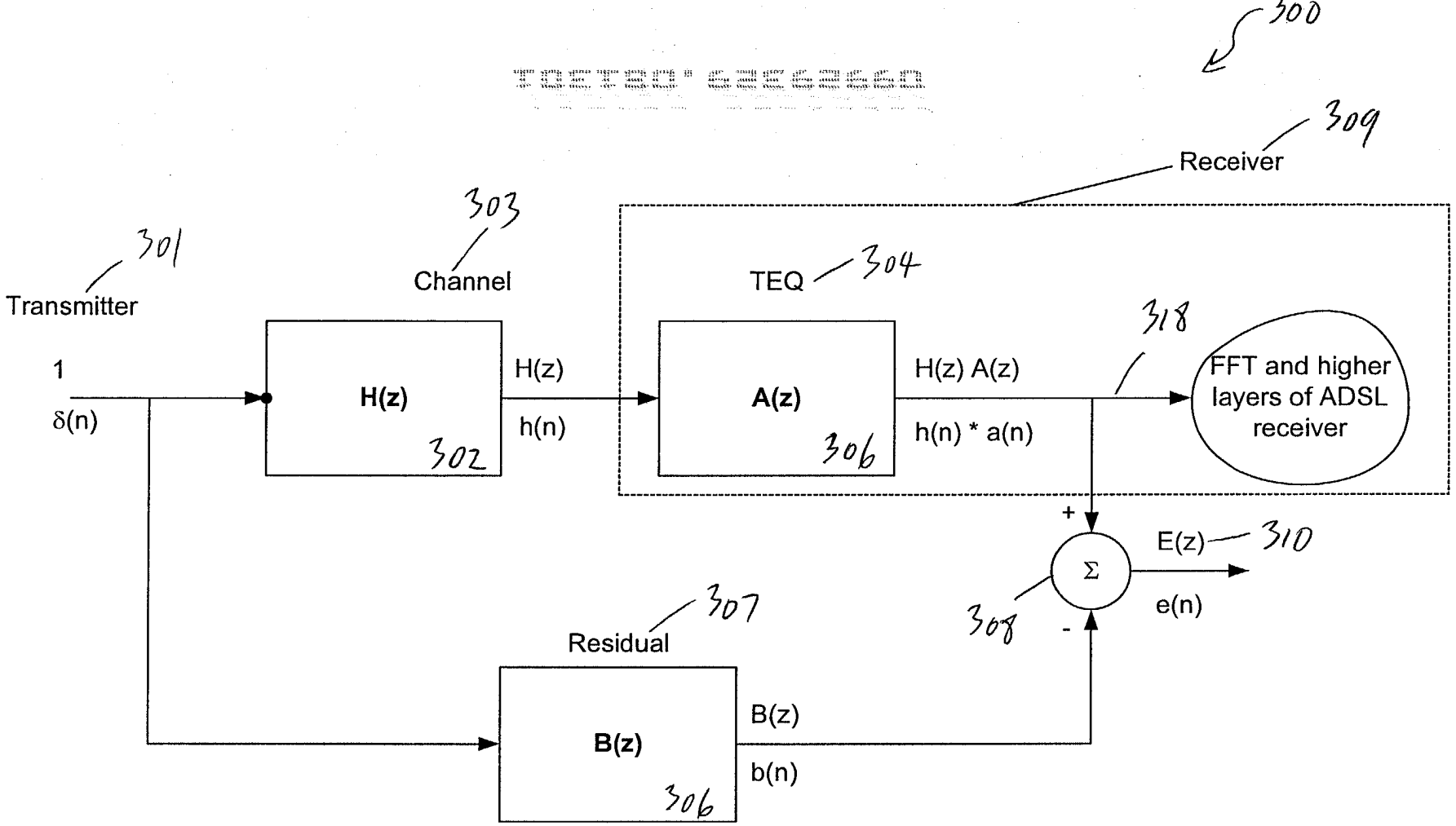
300
309
Receiver
303
Channel
301
Transmitter
TEQ
304
318
1
δ(n)
H(z)
302
H(z)
h(n)
A(z)
306
H(z) A(z)
h(n) * a(n)
FFT and higher layers of ADSL receiver
+
E(z)
310
Σ
308
e(n)
-
307
Residual
B(z)
306
B(z)
b(n)

Figure 3

General flow of steps

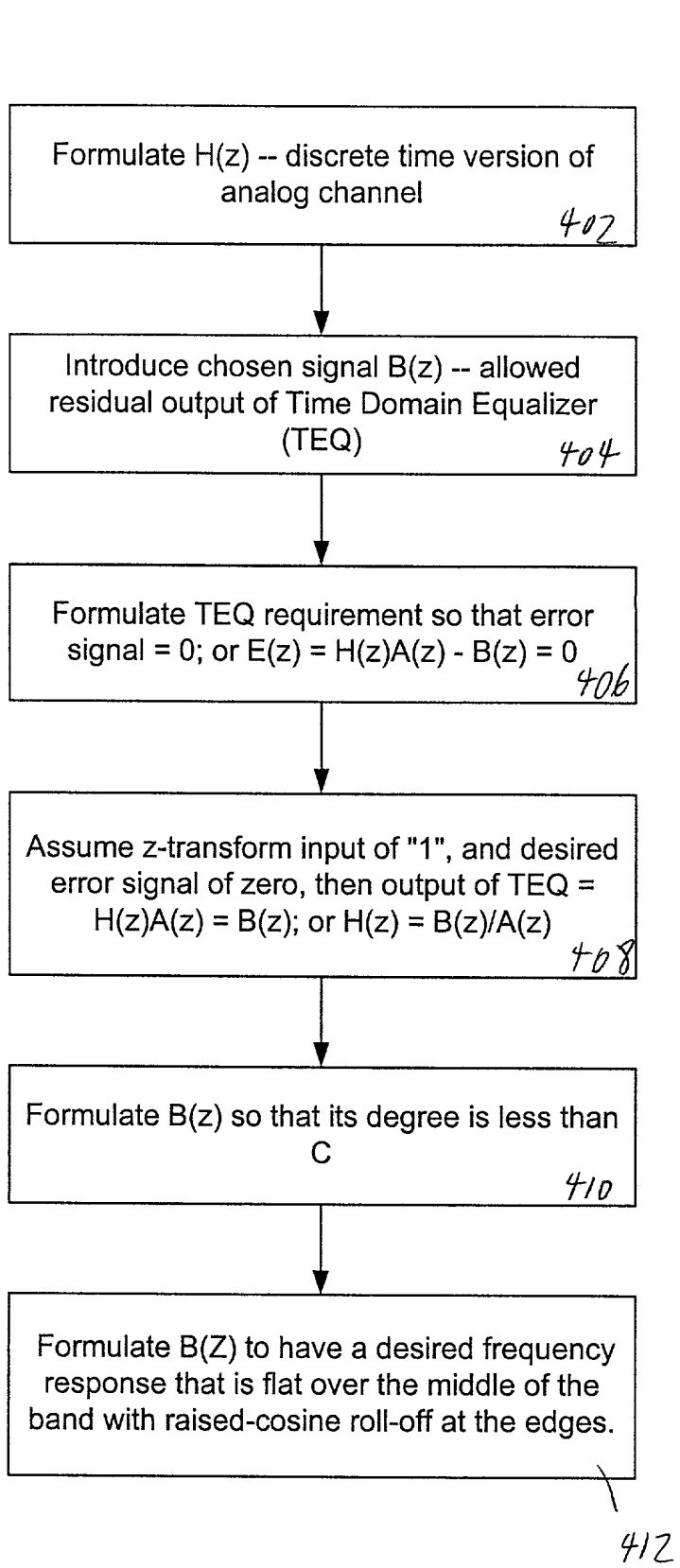

Figure 4

Formulate B(z)

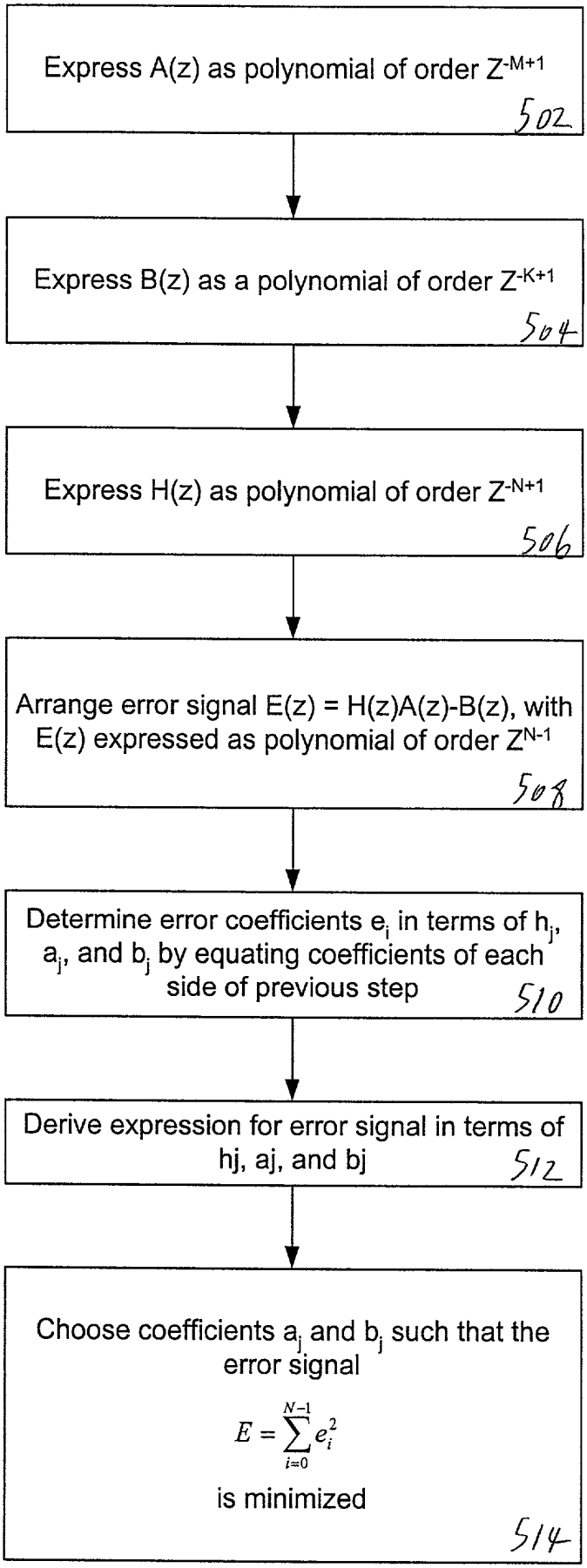

Figure 5

Minimize error signal

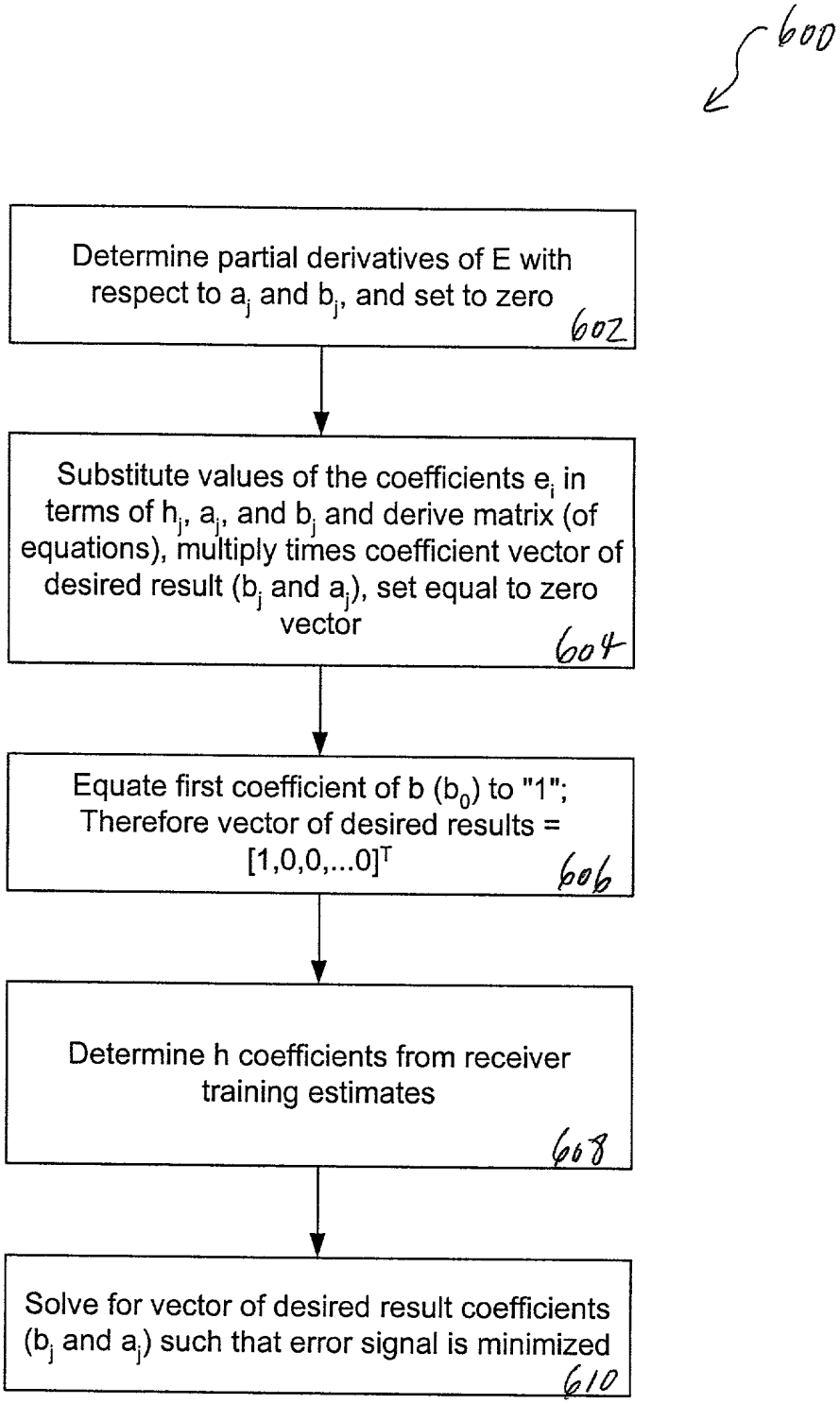

Figure 6